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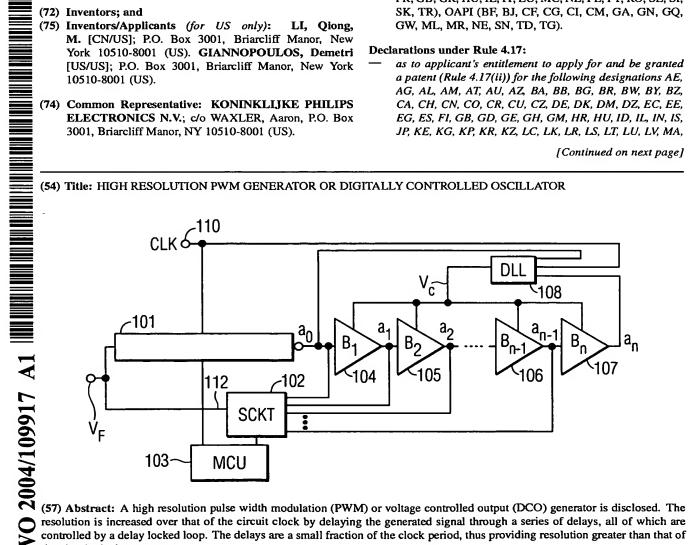
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resolution is increased over that of the circuit clock by delaying the generated signal through a series of delays, all of which are controlled by a delay locked loop. The delays are a small fraction of the clock period, thus providing resolution greater than that of the circuit clock.

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 as to the applicant's entitlement to claim the priority of the earlier application (Rule 4.17(iii)) for all designations

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